# Arc Fault Protection - Concept to Specification

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# Arc Fault Protection - Concept to Specification

- Background
- Concept
- Specification
- Test Method

# BACKGROUND

- 42 volt systems are being developed to meet ever growing power requirements
- 42 volt systems are more prone to sustained arcing than 12/14 volt system
- More sustained arcing environment may lead to the following issues:
  - loss of function of the affected circuit
  - loss of function of circuits with wiring in the proximity of the location of the arcing
  - increased fire hazard
  - direct personal injury at the location of the discharge of the arc energy
- As with the residential and aerospace industries, arcing can occur anywhere that:
  - insulation damage has occurred (enclosure impingement, chaffing, vibration, aging, maintenance)
  - the integrity of a connector has been compromised
  - exposed conductive power terminals have been bridged by foreign material
  - loose connections are bridged by arcs

# CONCEPT – Algorithm Development

Arc fault protection will minimize:

- the energy discharged by the arcing event
- the damage associated with the arc
- the likelihood and extent of personal injury/property damage

To accomplish this the arc fault protection must distinguish damaging arcs from:

- normal loads with chaotic components
- arcing associated with the normally operating equipment such as:
  - any opening or closing of mechanical contacts
  - motors with brushes

# CONCEPT – Algorithm Development

Algorithms must:

- be developed and proven with rigorous experimentation, based on a broad knowledge of the loads and faults expected on the circuits within the system to be protected.

- differentiate between the fundamental characteristics of the unwanted arcing and the acceptable arcing, and more chaotic loads.
  - an algorithm that relies heavily on special case identification of the more chaotic loads associated with normal system operation is fundamentally predisposed to a higher occurrence of nuisance interruptions or a lower sensitivity.

# CONCEPT - Prototype Hardware Development

The algorithm development must continue with further testing performed on flexible prototype hardware, with predictable performance during transition to firmer production hardware.

Essential

- Rapid assessment of algorithm and algorithm variable change
- Minimal susceptibility confounding
- Minimal translation error from analog to micro to PLD to ASIC, etc.

# SPECIFICATION – General Application Considerations

Strong link between the specification & application is essential to delivery of a product that delivers the highest possible value to any application.

A weak link:

- Does not cover as much of the application requirements as possible
  - predisposed to failure at some point in that application
- Invokes requirements that are not truly requirements of the application
  - adds cost to the product without adding any value to the product
- Each of these specification mistakes results in unnecessary cost to the end user.
  - Every specification is a compromise targeted at balancing a thorough specification that imposes only the performance characteristics that are related to the application that is to be served.

# SPECIFICATION – Algorithm Considerations

The algorithm should be developed at the same time that the specification is defined.

Simultaneous development reduces the likelihood of costly mismatches between the algorithm and the specification.

Some of the algorithm details that could effect arc fault technologies are:

- Response time
- Nuisance loads
- Coordination/cascading requirements
- Common Source Impedance Feedback
- Inductively Coupled Cross-Talk
- Physical distance to arc event

# SPECIFICATION - Arc Detection Considerations

The nature of the technology that detects arcs amplifies the difficulties associated with the best balance in a specification.

Arc fault technologies must account for highly variable arcing characteristics.

Such variations preclude any given arc fault technology from relying on physical characteristics such as luminescence, heat generation, rapid current rise, or even regularly occurring flat portions at the zero crossover of the alternating current wave.

- All of these conditions can be found on a normally operating system.

A successful working definition of arcing fault events must

- rely on the fundamental random nature of arcing
- combine this random nature with empirical knowledge of arcing fault event signatures that cause damage in the applications
- consider arcing that is common to a normally operating system, to minimize nuisance tripping this working definition

# SPECIFICATION - Arc Detection Considerations

One of the aspects of arc fault performance specification that is occasionally confusing is its reliance on the fundamental random nature of arcing events.

A performance-based specification relies on functional testing to characterize product performance as either acceptable to an application, or as not acceptable to that application.

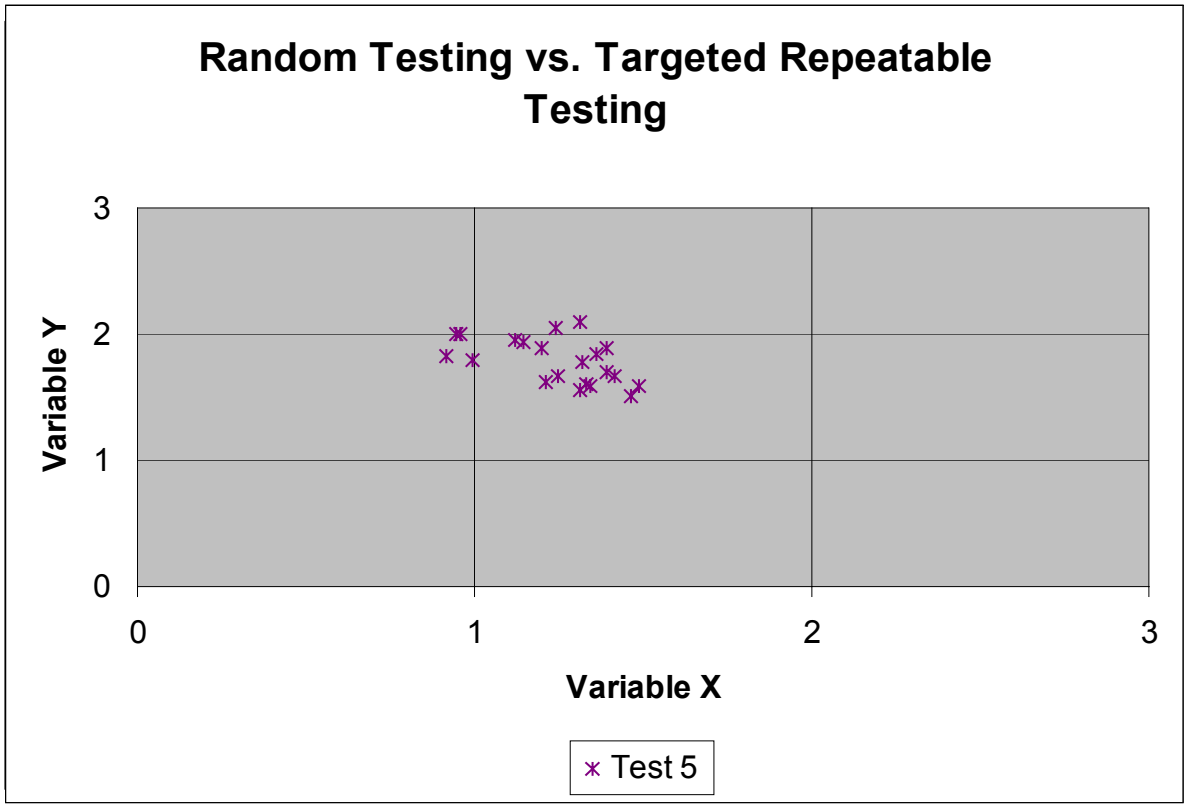
As with most products it is of paramount importance that this testing is as reproducible as possible.

The testing should be broad enough to cover the spectrum of conditions expected in the application, and no further.

The broad spectrum of testing necessary cannot be substituted by one highly variable test.

# SPECIFICATION

To illustrate this point please consider a two-dimensional performance model. In this performance model the worst case performance is experienced at the minimum and maximum for that dimension, in other words if it meets its specification requirements at X1 and X2 it will meet them at all points between X1 and X2.



# SPECIFICATION

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There is, of course a trade-off between the cost of decreasing the variability of the testing being conducted and the value of the decrease in variability realized.

It is especially important to keep this in mind with arc protection devices.

By its nature arcing is, potentially, extremely difficult to define. As such a realm of performance must be chosen, and well defined.

# TEST METHOD - General

There are three major categories of testing performed to characterize the performance of arc fault detection devices.

- arc detection tests
- nuisance load verification
- operation inhibition testing.

There are two major methodologies

- electronic or wave form testing
- live testing

# TEST METHOD – Wave Form Testing

Wave form testing captures current and voltage traces from arcing and nuisance load events performed in the application or in the lab. These traces are then replicated with a wave form generator and applied to the device under test. This approach can be used on the full device with full current and voltage, or it can be used to inject lower level signals into portions of the arc detection circuit.

Advantages

- speed of setup
- variety of performance parameters can be tested with one piece of equipment
- reduced variability

Disadvantages

- relatively large file sizes necessary to properly characterize the performance
- the method of control of this electronic data is not currently available
- technical concerns that even higher resolution data collection will not adequately capture the challenging characteristics of nuisance loads

These challenges aside, wave form testing will likely be part of every manufacturers internal acceptance test plans.

# TEST METHOD – Live Testing

Live testing exposes the DUT to actual arcing and nuisance load situations.

Technical Benefits

- the DUT is exposed to all of the characteristics of the arc or nuisance load.

Logistical Benefits

- live testing is much easier to specify than wave form testing

Disadvantages

- cumbersome to setup
- fairly inflexible
- highly variable
- sometimes even dangerous to conduct
- in some case live testing can also prove to be much more expensive & time consuming than wave form testing

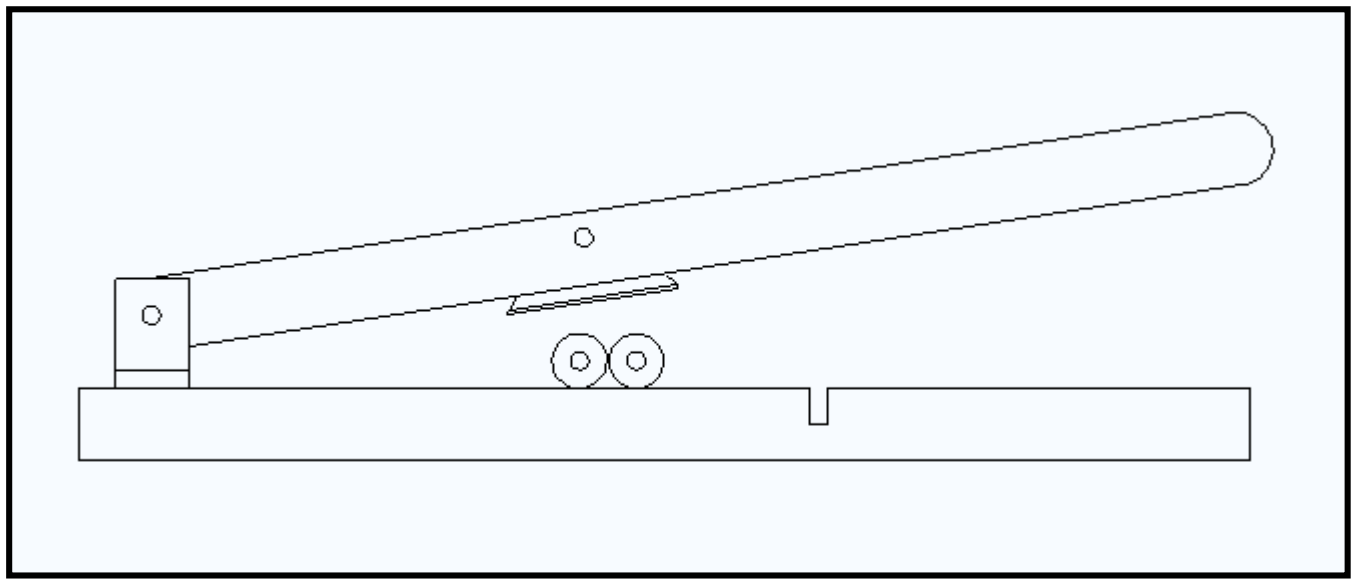
First releases of the residential and aerospace specifications have relied exclusively on this type of testing for demonstration of performance.

# TEST METHOD - Point Contact/Guillotine

The most recurring test for arc fault protection.

Simulate bridging by a metal conductor after insulation has chafed away.

A metal blade damages the insulation and bridges the gap between the conductors of two insulated wires at different potentials.



# TEST METHOD - Point Contact/Guillotine

Inexpensive to tool and to setup

Runs quick

Requires an oscilloscope record of the run to determine whether the DUT has met specification requirements.

Pass Fail Criteria

- typically defined in terms of clearing time
- commercial and aerospace AC specifications define clearing as a number of half cycles of arcing.

# TEST METHOD – Carbonized Path

Simulate conductive contamination bridging aged insulation.

During carbonized path testing the wire samples are first prepared as follows:

- the insulation is damaged on two insulated wires
- attach the two wires together, if not already integral, such that the damaged areas of insulation are adjacent
- impose a high potential across the two conductors, with the current limited to create a high resistance conductive path without excessive damage to the wire

These prepared samples are then exposed to line potentials, and various levels of available current, ranging from hundreds of amps to a fraction of the rated steady state current of the DUT.

Pass-Fail Criteria

- clearing times in number of cycles or in seconds
- must preclude ignition of a cotton fire indicator located adjacent to the fault in the wire sample

# TEST METHOD – Wet Arc

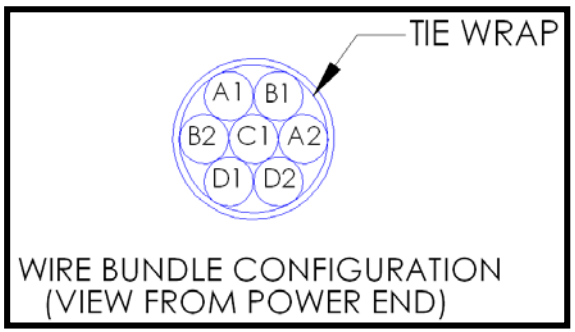
Simulate fluid electrolyte contamination of aged wiring.

Based on a wire insulation test, MIL-STD-2223, Method 3006

Uses a seven-wire wire bundle

The insulation on two of the wires is damaged, by removing the all of insulation on the full circumference

The windows of exposed conductor are then located axially separated by a distance of approximately 0.25 inches (6 mm)




# TEST METHOD – Wet Arc

The arc is then initiated by a slow drip of electrolytic solution of salt and water with a potential difference between the conductors of the two windowed wires

This test can be conducted at various potentials and available fault current.

Pass-Fail Criteria

- must preclude damage to the insulation of the other wires in the bundle - wet dielectric verification

# TEST METHOD – Loose Terminal

Simulate a loose screw type terminal connection

A number of loose terminal connections are installed between the DUT and a resistive load.

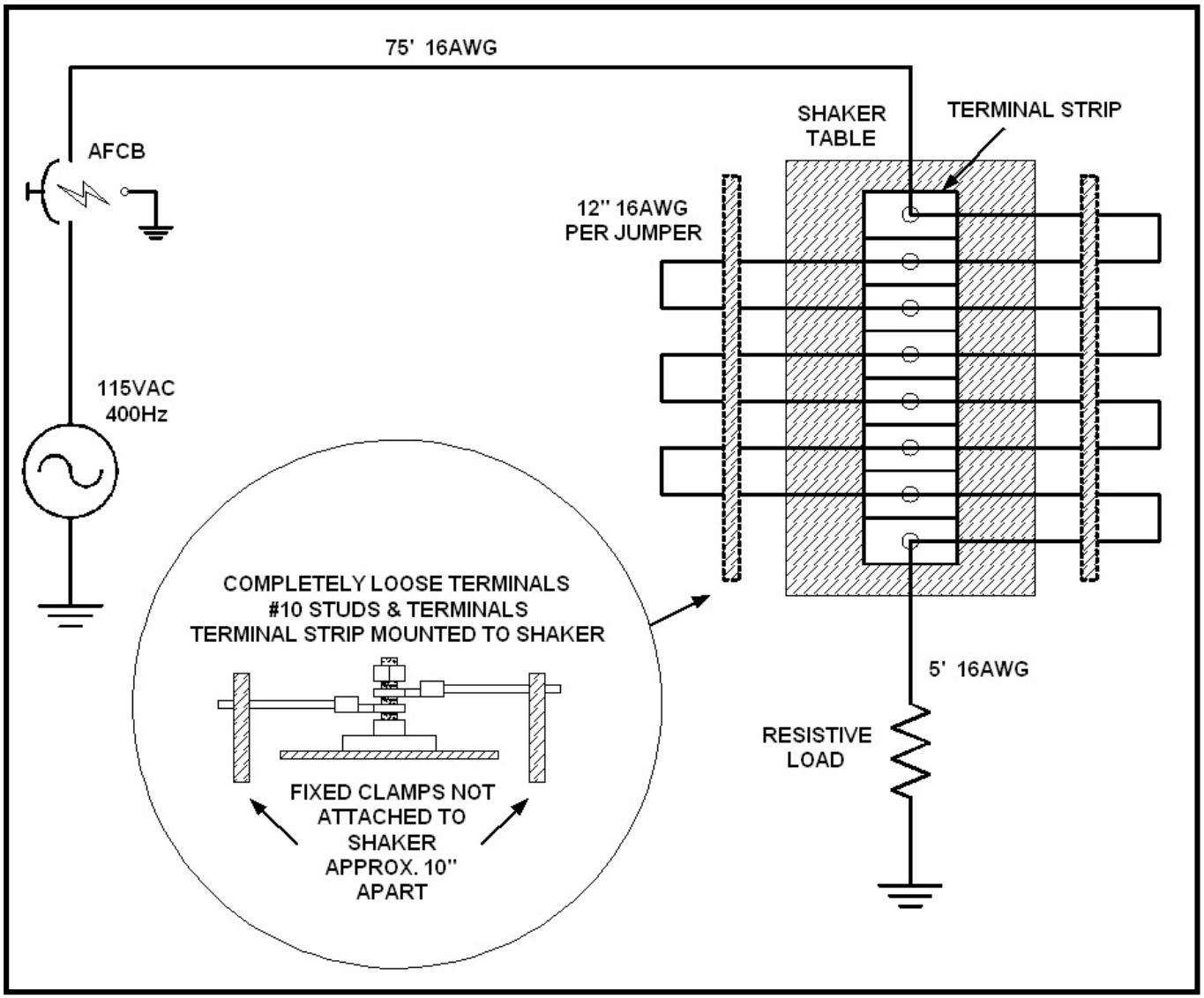
The array of loose terminals are then vibrated to simulate the vibration environment on the airplane, which initiates the arcing at each loose terminal

The current is limited to a fraction of the rated steady state current of the DUT

Pass-Fail Criteria

- the device must clear the arc within a period of time.

# TEST METHOD – Loose Terminal



# TEST METHOD – Arc Inhibition or Masking

A series of tests that insures that DUT can perform it's intended function in the application.

Runs most, if not all, of the arc detection testing required in combination with typical loads that will be experienced in application.

High amp testing is run in parallel with the masking load

Lower current testing is run with the arcing initiated in series with the masking load.

Pass-Fail Criteria

- Generally the same as the detection test being run

# CONCLUSION

Strong Link between Specification and Application

Wave Form vs. Live Testing

Library of Test Methods Available